

**AMENDMENTS TO THE CLAIMS**

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double-bracketed text indicating deletions.

1. (Currently Amended) An integrated burn-in test method for testing a multi-chip package, comprising:

~~loading the multi-chip package formed of multiple kinds of semiconductor devices, to a chamber of a burn-in equipment capable of applying a plurality of scan control clock signals;~~

uploading an integrated burn-in test program to the burn-in equipment for testing the multi-chip package; and

conducting a test of the multi-chip package using the integrated burn-in test program.

2. (Previously Presented) The method of claim 1, wherein the semiconductor device is a semiconductor package.

3. (Previously Presented) The method of claim 1, wherein the semiconductor device is a semiconductor chip.

4. (Previously Presented) The method of claim 1, wherein the multi-chip package performs a memory function.

5. (Previously Presented) The method of claim 1, wherein the test is conducted for each semiconductor device of the multi-chip package at a different temperature.

6. (Previously Presented) The method of claim 1, wherein the multi-chip package is loaded on a burn-in board and the burn-in board is loaded in the chamber of burn-in equipment.

7. (Previously Presented) The method of claim 1, wherein the multi-chip package is in the form of a TBGA (thin ball grid array).

8. (Previously Presented) The method of claim 1, wherein the integrated burn-in test program uses a multiplexer selection function for applying a desired test condition during testing of each semiconductor device.

9. (Previously Presented) The method of claim 1, wherein the integrated burn-in test program has an I/O masking function for blocking some I/O terminals.

10. (Previously Presented) The method of claim 1, wherein the integrated burn-in test program has a function of setting a burn-in temperature condition for different kinds of semiconductor devices.

11. (Currently Amended) The method of claim 6, wherein after loading the multi-chip package on the burn-in board to a ~~the~~ chamber of the burn-in equipment, a contact test is conducted to examine whether an electrical connection of the burn-in board is correct.

12. (Previously Presented) The method claimed in claim 1, wherein the burn-in test is a monitoring burn-in test.

13. (Previously Presented) The method of claim 1, wherein the integrated burn-in test program requires only one time bin sorting based on the burn-in test result.

14. (Currently Amended) An integrated burn-in test method for testing a multi-chip package, comprising:

~~loading the multi chip package including different kinds of semiconductor devices on a burn in board;~~

~~loading the burn in board into a chamber of a burn in equipment capable of applying a plurality of scan control clock signals;~~

uploading an integrated burn-in test program to test different kinds of semiconductor devices to ~~the~~ burn-in equipment;

conducting a contact test for a ~~the~~ burn-in board to examine an electrical connection;

conducting a burn-in test for the different kinds of semiconductor devices using a multiplex selection function of the integrated burn-in test program loaded to the burn-in equipment;

ending the burn-in test for different kinds of semiconductor devices; and

bin sorting the multi-chip package based on the burn-in test result.

15. (Previously Presented) The method of claim 14, wherein when burn-in test for different kinds of semiconductor devices are performed sequentially and the integrated burn-in test program controls the chamber temperature according to a test temperature for an individual semiconductor device.

16. (Previously Presented) The method of claim 14, wherein each semiconductor device performs a memory function.

17. (Currently Amended) The method of claim 14, wherein the integrated burn-in test program has an I/O masking function for blocking some I/O terminals.

18. (Previously Presented) The method of claim 17, wherein each semiconductor device of the multi-chip package has a different number of I/O terminal pins.

19. (Previously Presented) The method of claim 14, wherein the multi-chip package is in the form of a TBGA (thin ball grid array).

20. (Previously Presented) The method of claim 14, wherein the burn-in test is a monitoring burn-in test.

21. (Previously Presented) An integrated burn-in test method for testing a multi-chip package, comprising:

providing the multi-chip package formed of multiple types of semiconductor device; and

testing the multi-chip package with an integrated burn-in test program.

22. (Previously Presented) The method of claim 21, wherein the testing includes applying a specific test condition during testing of each semiconductor device, wherein the specific test condition is defined by a multiplexer selection function.

23. (Previously Presented) The method of claim 21, wherein the testing includes blocking some I/O terminals during testing of some semiconductor devices, wherein the blocking is defined by an I/O masking function.

24. (Previously Presented) The method of claim 21, wherein the testing includes setting a specific burn-in temperature condition for different types of semiconductor devices.

25. (Previously Presented) The method of claim 21, wherein the testing includes performing a contact test once for all different types of semiconductor devices of the multi-chip package.

26. (Previously Presented) The method of claim 21, further comprising:

bin sorting once for all different types of semiconductor devices of the multi-chip package based on the testing result.

27. (Previously Presented) An integrated burn-in test method for testing a multi-chip package, comprising:

providing the multi-chip package formed of multiple types of semiconductor device;  
testing the multi-chip package with an integrated burn-in test program, including  
performing a contact test once for all different types of semiconductor

devices of the multi-chip package,  
blocking some I/O terminals during testing of some semiconductor devices,  
wherein the blocking is defined by an I/O masking function,  
setting a specific burn-in temperature condition for different types of  
semiconductor devices,

conducting a burn-in test for the multiple types of semiconductor devices by  
applying a specific test condition for each semiconductor device, wherein the specific  
test condition is defined by a multiplexer selection function; and

bin sorting once for all different types of semiconductor devices of the multi-chip package  
based on the testing result.

28. (New) The method of claim 1, further comprising:

loading the multi-chip package formed of multiple kinds of semiconductor  
devices, to a chamber of the burn-in equipment capable of applying a plurality of scan  
control clock signals.

29. (New) The method of claim 14, further comprising:

loading the multi chip-package including different kinds of semiconductor devices on the burn-in board; and

loading the burn-in board into a chamber of the burn-in equipment capable of applying a plurality of scan control clock signals.